High aspect ratio InGaAs FinFETs with sub-20 nm fin width

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Abstract

We demonstrate self-aligned InGaAs FinFETs with sub-20 nm fin width fabricated through a CMOS compatible front-end process. Working devices with fins as narrow as 7 nm, fin aspect ratios in excess of 5 and gate lengths as short as 20 nm have been fabricated using precision dry etching and digital etch. The devices also feature self-aligned metal contacts that are 20-30 nm away from the edge of the gate. FinFETs with L_g=30 nm, W_f=22 nm and channel height of 40 nm exhibit a transconductance of 1400 μS/μm at V_{DS}=0.5 V. When normalized to W_f, this is a record value among all III-V FinFETs, indicating that our device architecture makes efficient use of conduction along the fin sidewalls.

Introduction

InGaAs is a promising candidate as channel material for CMOS technologies beyond the 10 nm node [1]. In this dimensional range, only high aspect-ratio (AR) 3D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive fin and nanowire based InGaAs FinFET prototypes have recently been demonstrated [2-4]. However, to date, InGaAs FinFETs with fin widths below 30 nm and channel aspect ratio better than unity have yet to be demonstrated. Furthermore, the channel sidewall slopes demonstrated so far are typically lower than 80^0. At the point of insertion in a sub-10 nm node, InGaAs FinFETs with sub-10 nm fin widths and steep sidewalls will be required.

In this work, we present the first self-aligned InGaAs FinFETs with sub 20-nm fin width, high channel aspect ratio, vertical sidewalls, gate lengths as short as 20 nm and CMOS-type manufacturability. For this, we use a top down process based on a combination of RIE and digital etch. Our transistors are the most aggressively scaled InGaAs FinFETs to date.

Process Technology

Our fabrication process closely follows CMOS requirements, particularly self-alignment of the refractory metal gate and metal contacts, very low thermal budget, gate-last process that uses RIE extensively and an entirely lift-off free process in the front end.

The starting heterostructure is shown in **Fig. 1**. It is grown by MBE and it features a H_c=40 nm thick InGaAs channel layer and an n^+ InGaAs cap. The process is illustrated in **Fig. 2** and follows a flow developed for self-aligned planar InGaAs Quantum-Well MOSFETs [5]**.** SEM images of sub-20 nm fin test structures are shown in **Fig. 3**. **Figs. 4-5** show SEM images of FinFETs at different steps in the process.

Low-ρ Mo is first sputtered as contact metal (R_{sh}=5 Ω/□), followed by SiO_2 CVD. The gate pattern is defined by E-beam lithography. The SiO_2 and Mo layers are then etched by RIE. After RIE mesa isolation, the top n^+ InGaAs cap is wet-etched in a well-controlled manner that yields an undercut of ~20 nm (**Fig. 4**). Fins are then patterned using 40 nm thick HSQ and E-beam lithography and RIE etched using a $BCl_3/SiCl_4/Ar$ chemistry [6]. This yields fins as narrow as 20 nm with an H_f/W_f (Fig. 2) aspect ratio of 8. The fins are highly vertical in the top ~70 nm (**Fig. 3**). To further thin down the fins and smooth the sidewalls, we perform digital etch cycles [7].

Immediately after the last digital etch cycle, 0.5 nm of Al_2O_3 and 2.5 nm HfO_2 are deposited by ALD (EOT~1 nm). Sputtered Mo is used as gate metal and patterned by RIE. The device is finished by via opening and pad formation. This is the only lift-off step at the backend of the process. The final gate length is defined by the recess opening in the SiO_2 which can reach below 20 nm. In this process, the HSQ that defines the fin etch is kept in place. This makes our FinFETs double-gate transistors with carrier modulation only on the sidewalls.

Transistor Results

The electrical characteristic of a device with W_f=22 nm and L_g= 600 nm are shown in **Fig. 6**. Well-behaved long-channel characteristics and good sidewall control are obtained. **Fig. 7** shows electrical characteristics of a W_f=22 nm (AR= H_c/W_f=1.8), L_g=30 nm device. Its R_{on} is 180 Ω·μm and a peak g_m of 1400 μS/μm is obtained at V_{DS}=0.5 V. This value is comparable to the highest g_m obtained so far in InAs FinFETs with W_f=40 nm (AR=0.23) [8]. The subthreshold characteristics of our device indicate a subthreshold swing, S, of 170 mV/dec and DIBL of 220 mV/V at 0.5 V (**Fig. 8a**). **Fig. 8b** shows the subthreshold and output characteristics of the most aggressively scaled device obtain in this work with W_f=7 nm (AR=5.7) and L_g= 20 nm. Well behaved characteristics are demonstrated. Consistent with the double-gate nature of our devices, all figures of merit have been normalized by two times the channel height.

Discussion

Fig. 9 shows R_{on} as a function of L_g for different W_f. R_{sd}~100 Ω·μm for all W_f is obtained. This excellent value emerges from the self-aligned design. **Fig 10** shows V_T (1 μA/μm at V_{DS}=50 mV) as a function of L_g for different W_f. While for W_f=22 and 17 nm a classic V_T rolloff is observed, for W_f=12 nm a strong dependence over the entire L_g range is visible. We attribute this to line edge roughness which affects thin long fins [9]. This effect is also enhanced due to quantum size effects [10]. g_{m_max}, S, and I_{on} as a function of L_g for different W_f are shown in **Fig. 11**. A clear tradeoff between g_m and S emerges, which governs the L_g at which maximum I_{on} (at a fixed I_{off}=100 nA/μm and V_{DD}=0.5 V) is obtained. As the fins become narrower, I_{on} peaks at shorter L_g while $g_{m,max}$ and S_{min} also degrade. We attribute this is to the increased effect of sidewall scattering and suggests further work is needed.

As a benchmark of our results, **Fig. 12** shows peak g_m normalized to the fin width as a function of W_f for InGaAs FinFETs from the literature and our own. This FOM emphasizes the importance of maximizing current drive in very thin fins. Our InGaAs FinFETs are the first to feature sub-30 nm W_f and they also exhibit the highest g_m per fin footprint to date.

Conclusions

We demonstrate the first self-aligned InGaAs FinFETs with W_f<30 nm and channel aspect ratio as high as 6. Fully operational devices with fin widths as narrow as 7 nm and sub-30 nm gate lengths are demonstrated. A record g_m per fin footprint has been achieved.

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References: [1] J. A. del Alamo, *Nature,* 479, 317 (2011). [2] M. Radosavljevic et al., *IEDM* 2011, p. 765. [3] T-W._Kim et al., *IEDM* 2013, p. 415. [4] A. Thathachary et al., *VLSI* 2015. [5] J. Lin *et al., IEDM* 2013, p. 421. [6] X. Zhao *et al., IEDM* 2013, p. 695. [7] J. Lin *et al., EDL 35(4) 440 (2014).* [8] S-H Kim et al., *TED* 61(5), 1354 (2014). [9] J. B. Chang, *VLSI* 2011. [10] A. Vardi et al., *IEDM* 2015, p. 807.

Fig. 1: Starting heterostructure.

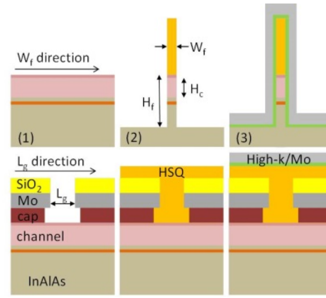

Fig. 2: Left: process flow. Right: device schematics at the points in the process marked by numbers.

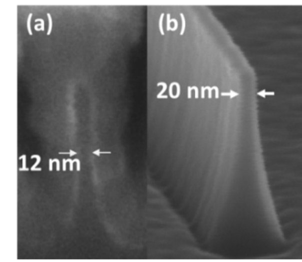

Fig. 3: InGaAs fins in this work: (a) cross-section, (b) stand alone.

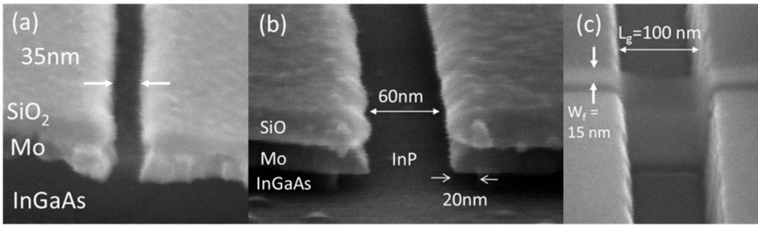

Fig. 4: SEM images of transistors in process: (a) after dry recess, (b) after wet recess, and (c) after fin etch.

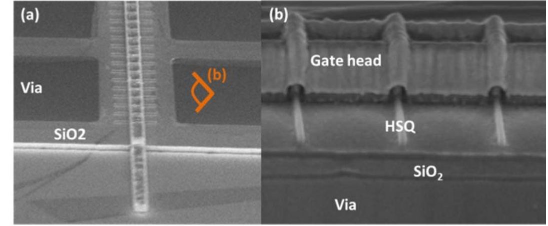

Fig. 5: SEM images from back end after gate patterning and via opening. (b) view marked in (a).

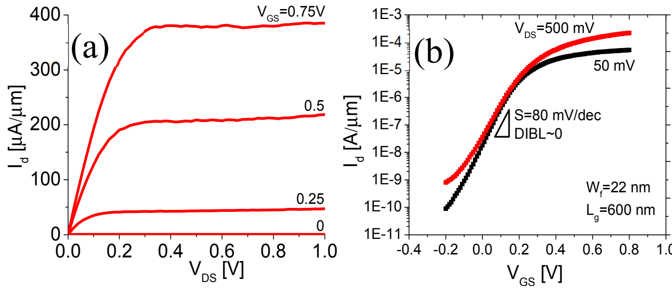

Fig. 6: Output (a) and subthreshold (b) characteristics of FinFET with W_f=22 nm and L_g=600 nm.

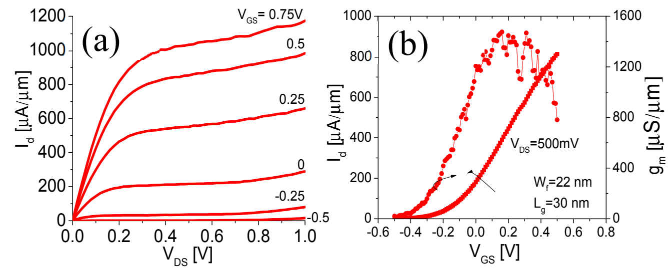

Fig. 7: Output (a) and transfer (b) characteristics of device with W_f=22 nm and L_g=30 nm.

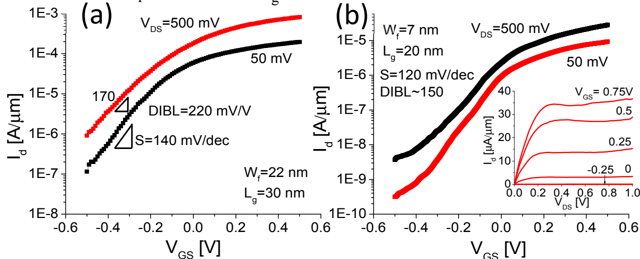

Fig. 8: Subthreshold characteristics of (a) W_f=22 nm, L_g=30 nm and (b) W_f=7 nm, L_g=20 nm devices. Inset of (b): output characteristics of the same device.

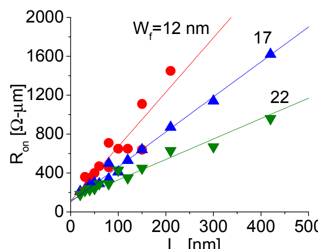

Fig. 9: R_{on} as a function of L_g for different W_f.

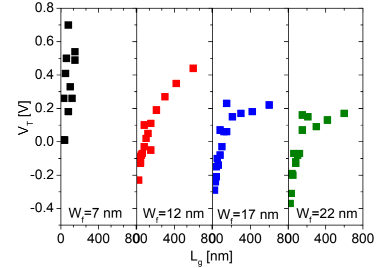

Fig. 10: V_T at 1 μA/μm and V_{DS}=50 mV as a function of L_g for different W_f.

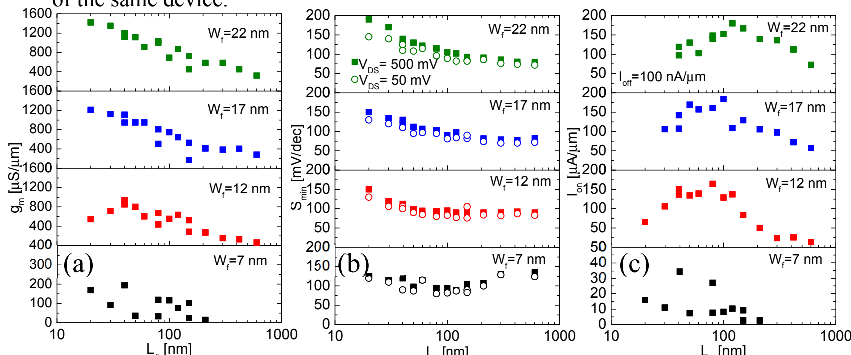

Fig. 11: From left to right: g_m at V_{DS}=0.5 V, S_{min} (linear and saturated), and I_{on} (at I_{off}=100 nA/μm and V_{DD}=0.5 V) as a function of L_g for different W_f.

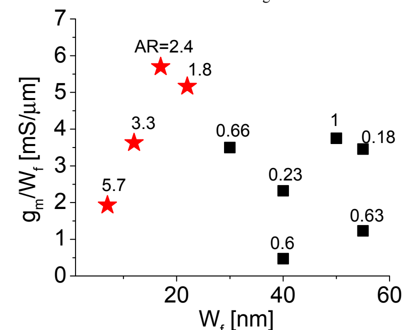

Fig. 12: Benchmark of g_m per fin footprint vs. W_f for InGaAs FinFETs in the literature (black squares) and this work (red stars). Each data point is labeled with the channel AR=H_c/W_f.